



Logic Portfolio
Voltage translators / Level shifters

Introduction

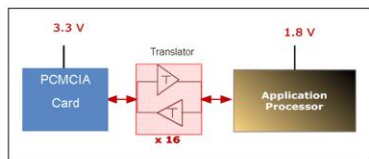
- ▶ Purpose: Explain the voltage/level translation techniques, NXP's voltage translation portfolio and applications.
- ▶ Objective: Understand the theory, features, applications and selection of voltage level translators from NXP.
- ▶ Content: 22 Pages
- ▶ Learning Time: 20 Minutes



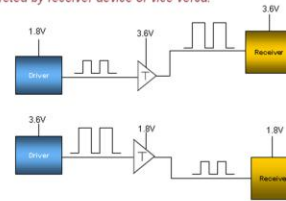
Welcome to NXP's voltage translators training module. This module will explain the techniques and features of NXP's voltage translators. The module will also help to select the right voltage translator for specific applications.

Voltage translation: why?

- ▶ New designs/applications use lower supply voltage i.e. 3.0V or lower
- ▶ All the devices used in a design/application do not use same supply voltage
- ▶ A newly designed CPU, uses a lower voltage e.g. 1.8V but a proven old peripheral uses higher supply voltage e.g. 3.3V. Memory devices, image sensors, PCMCIA cards, RF transceivers are some peripheral examples
- ▶ To prevent the current flow in mismatched voltage supplies

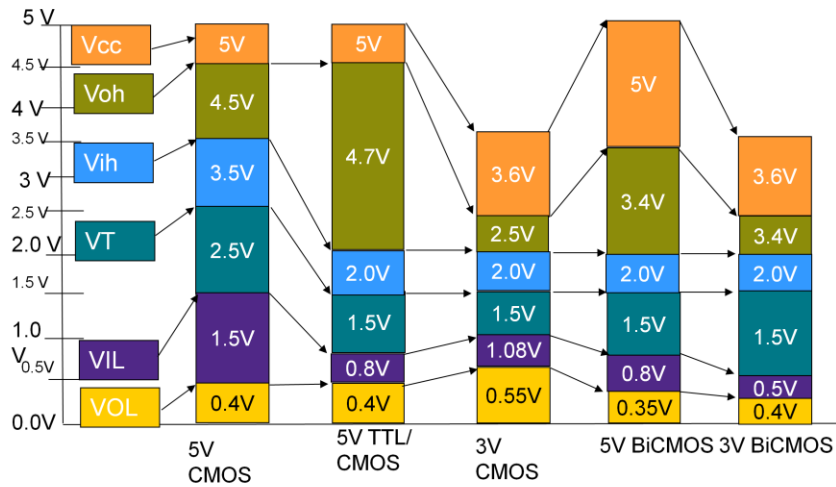


" In logic devices, voltage translation means that the output voltage level of driver device needs to be shifted up or down so that it can be correctly interpreted by receiver device or vice versa."



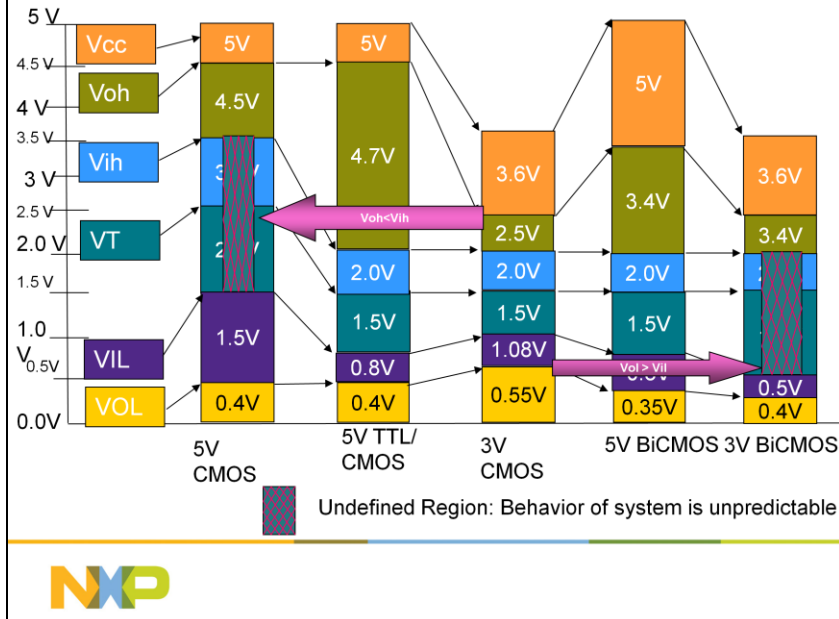
Voltage translation is required to ensure that devices operating at different supply voltages in a system are able to work with each other without any damaging current flow and signal loss.

Logic Switching Threshold and Output Levels



Input switching threshold and output voltage levels for 5V/3V CMOS, mixed CMOS/TTL and BiCMOS logic families are shown here. High level output voltage (V_{oh}) of driver device must be higher than high level input threshold voltage (V_{ih}) of receiver device and the low level output voltage (V_{ol}) of driver must be lower than low level input threshold voltage (V_{il}) of receiver for proper working of CMOS devices.

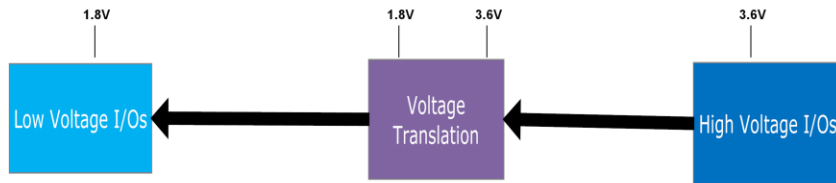
Logic Threshold and Output Levels



However, if V_{OH} of driver is lower than V_{IH} of receiver and/or V_{OL} of driver is higher than V_{IL} of receiver, the system behavior becomes unpredictable as shown in this slide. Therefore, it is necessary to match the input switching thresholds of receiver with output voltage levels of driver in a mixed voltage system.

Theory of Voltage Translation

Hi to Lo Voltage Translation



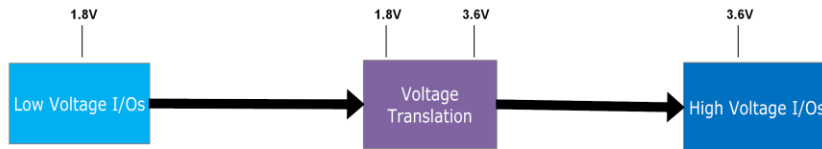
- ▶ Input pins of receiving device must be overvoltage tolerant for Hi-Lo level translation
- ▶ There is no damaging current flow from high voltage driver to low voltage inputs
- ▶ By using current limiting resistors at the inputs of CMOS devices, high to low voltage translation can be done.



If inputs of receiving device are over supply voltage tolerant, they can accept the input signals which are higher than the supply voltage. Since the outputs of such devices are referenced to V_{cc} , high to low voltage translation becomes possible. Use of current limiting resistors with CMOS devices which have diodes between inputs and V_{cc} is another technique for high to low voltage translation.

Theory of Voltage Translation

Low to High Voltage Translation



- ▶ Open drain/ collector outputs of a translator can be pulled up to the desired voltage level in low to high voltage translation
- ▶ Devices with input switching thresholds lower than typical, can also be used for low to high voltage translation

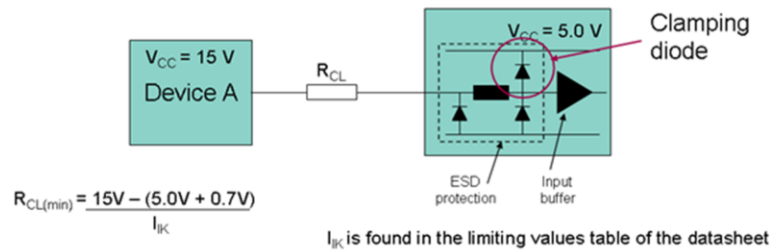


Open drain outputs and low input switching thresholds of CMOS devices are common techniques for low to high voltage translation.

Theory of Voltage Translation

▶ Current Limiting Resistors

By using current limiting resistors at the inputs of CMOS devices, the input voltages can be exceeded from maximum specified values, if maximum current rating is observed. Therefore, high to low voltage translation can be done, when proper current limiting resistors are used.

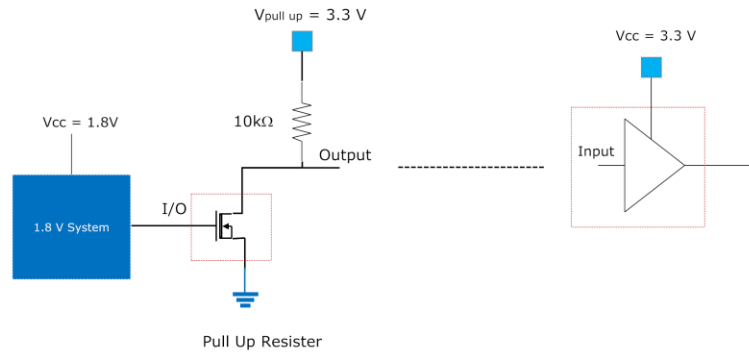


Use of current limiting resistors in CMOS devices for high to low voltage translation is explained in this slide. Value of required current limiting resistor can be calculated by using Vcc values of driver and receiver devices and allowed input clamping current for receiver as shown here.

Theory of Voltage Translation

► Open Drain Outputs

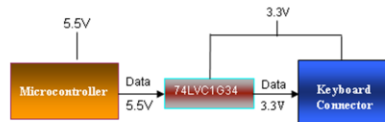
Open drain outputs of transistors can be used to translate the output voltage to a specific/desired operating voltage level and drive the next stage.



A pull up resistor can be used with the open drain outputs of standard logic functions to implement the low to high voltage translation and drive the next device as shown in this slide.

NXP's High to Low Voltage Translators

Choose a device with over-voltage tolerant inputs



- ▶ LVC, LVT, ALVT and AHC/T devices have over-voltage tolerant inputs up to 5.5V and can be used for HIGH to LOW voltage translation
- ▶ Inputs of AUP and AVC devices are tolerant up to 3.6V only. They are suitable for 1.8V/3.3V mixed designs
- ▶ LV, HC and HEF devices have input clamping diodes to V_{CC} and can be used with current limiting resistors for HIGH to LOW voltage translation
- ▶ Examples:

Part Number	How	Description	Vcc Range
74AUP2G157	Overvoltage tolerant inputs	Low Power 2 input Multiplexer	0.8V - 3.6V
74LV00	Current Limiting Resistor	Quad 2 Input NAND Gate	1V - 5.5V
74AVC16373	Overvoltage tolerant inputs	16 bit transparent D type latch	1.2V - 3.6V
74ALVC74	Overvoltage tolerant inputs	Dual D Type Flip Flop with Set and Reset	1.65V - 3.6V
74LVC3G34	Overvoltage tolerant inputs	Triple Buffer Gate	1.65V - 5.5V
74AHC1G86	Overvoltage tolerant inputs	2 Input Exclusive OR Gate	2V - 5.5V
74HC2G02	Current Limiting Resistor	Dual 2 Input NOR Gate	2V - 6V
74HC4049	Overvoltage tolerant inputs	Hex Inverting Hi-Lo Level Translator	2V - 6V
74HC4050	Overvoltage tolerant inputs	Hex Inverting Hi-Lo Level Translator	2V - 6V
74ALVT162244	Overvoltage tolerant inputs	16 Bit Buffer Driver with 30 Ohm Termination Resistors	2.3V - 3.6V
74LVT240	Overvoltage tolerant inputs	Octal Inverting Buffer	2.7V - 3.6V
HEF4049B	Overvoltage tolerant inputs	Hex Inverting Hi-Lo Level Translator	3V - 15V
HEF4104B	Overvoltage tolerant inputs	Quad Hi-Lo level Translator with 3 State Outputs	3V - 15V
HEF4050B	Overvoltage tolerant inputs	Hex Non-Inverting Hi-Lo Level Translator	3V - 15V



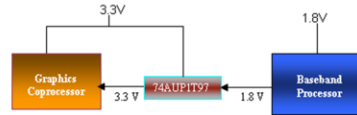
10

NXP's LVC, LVT, ALVT and AHC/T devices have over-voltage tolerant inputs up to 5.5V and can be used for HIGH to LOW voltage translation in 5V/3.3V mixed supply voltage systems. Inputs of AUP and AVC devices are tolerant up to 3.6V only. They are suitable for 1.8V/3.3V mixed designs. LV, HC and HEF devices can be used with current limiting resistors for HIGH to LOW voltage translation for interfacing with voltages far in excess of typical logic families.

NXP's Low to High Voltage Translators

Choose a device with low threshold inputs or open-drain outputs

Examples:




Part Number	How	Description	Vcc Range
74AUP1T57	Low Threshold Inputs	Single Low Power Configurable multiple function	0.6V - 3.6V
74AUP1T58	Low Threshold Inputs	Single Low Power Configurable multiple function	0.6V - 3.6V
74AUP1T97	Low Threshold Inputs	Single Low Power Configurable multiple function	0.6V - 3.6V
74AUP1T98	Low Threshold Inputs	Single Low Power Configurable multiple function	0.6V - 3.6V
74AUP1G07	Open Drain Outputs	Single Low Power Buffer	0.8V - 3.6V
74AUP2G07	Open Drain Outputs	Dual Low Power Buffer	0.8V - 3.6V
74AUP1G38	Open Drain output	Single Low Power 2 Input NAND Gate	0.8V - 3.6V
74AUP2G38	Open Drain Outputs	Dual Low Power 2 Input NAND Gate	0.8V - 3.6V
74AUP1G06	Open Drain outputs	Single Low Power Inverter	0.8V - 3.6V
74LV03	Open Drain Outputs	Quad 2 Input NAND Gate	1V - 5.5V
74AUP1T34	Low Threshold Inputs	Single Low Power Dual Supply Buffer	1.1V - 3.6V
74LVC38A	Open Drain Outputs	Quad 2 Input NAND Buffer	1.2V - 3.6V
74LVC2G06	Open Drain Outputs	Dual Open Drain Inverter	1.2V - 3.6V
74HCT1G08	Low Threshold Inputs	Single 2 Input AND Gate	4.5V - 5.5V
74HCT1G86	Low Threshold Inputs	Single 2 Input Exclusive OR Gate	4.5V - 5.5V
74HCT2G17	Low Threshold Inputs	Dual non inverting schmitt trigger	4.5V - 5.5V
74AHCT1G79	Low Threshold Inputs	Single D type flip flop	4.5V - 5.5V
74AHCT245	Low Threshold Inputs	Octal Bus Transceiver	4.5V - 5.5V
74LVC07A	Open Drain Outputs	Hex Buffer	1.65V - 5.5V
74LVC2G38	Open Drain Outputs	Dual 2 Input NAND Buffer	1.65V - 5.5V
74AHC1G09	Open Drain Outputs	Single 2 Input AND Gate	2V - 5.5V
74HCT3G07	Low Threshold Inputs and Open Drain Outputs	Triple Open Drain Buffer	4.5V - 5.5V
74HC03	Open Drain Outputs	Quad 2 Input NAND Gate	2V - 6V



NXP's AUPxT and HCT logic have lower than typical input switching thresholds and can be used for low to high voltage level translation. AUP1T57, AUP1T58, AUP1T97, AUP1T98 (1.8V to 3.6V) and HCT logic devices fall in this category. 03, 06, 07, 09, 11, 38, 7273, 9114, 9115 are the functions with open drain outputs in HC/T, LV, AHCT, AUP, LVC and FAST logic families.

Family Specifications Comparison

AUP	LVC	AVC
<ul style="list-style-type: none"> V_{CC}: 0.8 – 3.6V High Speed (~ 2ns prop delay) Static Output drive of +/-4mA* 3.6 V tolerant I/Os Schmitt Trigger action at Inputs Low Threshold Inputs Options High impedance suspend mode 3 State Outputs and open drain outputs Ioff circuit for partial power down/stand by mode operation Lowest power consumption / Ideal for battery powered devices RoHS compliant and Halogen free PicoGate and MicroPak packages -40 C to 125 C Operating Temperature Range 	<ul style="list-style-type: none"> V_{CC}: 1.2V – 5.5V ~4 ns prop delay Static Output drive of +/-24mA* Schmitt Trigger action at inputs and 5V Tolerant I/Os Open Drain Outputs option High impedance suspend mode 3 State Outputs Live Insertion Bus Hold and Termination Resistors option Flow Through Pin out** and Minimum Ground Bounce RoHS compliant and Halogen Free SO, TSSOP, PicoGate, DQFN and MicroPak Packages -40 C to 125 C Operating Temperature Range 	<ul style="list-style-type: none"> V_{CC}: 1.2V – 3.6V High Speed (~ 2ns prop delay) Static output drive of ±12 mA drive* Schmitt Trigger action at inputs Low Threshold Inputs Low Input Capacitance (typically 1pF) 3.6V Overvoltage tolerant I/Os 3 State Outputs Optional Bus Hold function High Impedance Suspend Mode Power off disabled outputs for Live Insertion RoHS and Halogen free TSSOP and TVSOP packages -40 C to 125 C Operating Temperature Range
		
<p>* At V_{CC} = 3V</p> <p>** For Voltage Translators and Transceivers functions Only</p>		
		12

Wide voltage translation range, low propagation delays, and different drive currents are available in AUP, LVC and AVC voltage translators from NXP. With the low I_{CC} and I_{off} in partial power down mode, these devices consume very low power in active and standby modes. Optional bus hold and integrated termination resistors can reduce the external components saving board space and cost. PicoGate is a very small 5, 6 or 8 pin TSSOP package with leads and MicroPak is the leadless smaller package. DQFN is the world's smallest leadless package for full function logic devices.

Family Specifications Comparison


AHC/T	HC/T	HEF4000B
<ul style="list-style-type: none"> Vcc: 2V – 5.5V 5 ns prop delay Static output drive of ± 8 mA TTL compatible inputs Schmitt Trigger action at inputs 3 State Outputs 5.5V Overvoltage tolerant I/Os for mixed 3.3V/5V designs RoHS and Halogen free SO, SSOP and TSSOP, PicoGate and leadless MicroPak packages Extended Operating Temp. range of -45 C to 145 C 	<ul style="list-style-type: none"> Vcc: 2-6V 9 ns prop delay Static output drive of ± 8 mA Input Clamping Diodes Low Threshold Inputs Option 3 State Outputs Open Drain outputs Option NXP has Largest Portfolio in Industry RoHS and Halogen Free SO, SOP and TSSOP and leadless DQFN packages Wide temperature range of -4C – 125 C 	<ul style="list-style-type: none"> Vcc: 5V – 15V 60 ns prop delay Static output drive of ± 3 mA* Input Clamping Diodes High fan out capability 3 State Outputs RoHS and Halogen Free TSSOP, SO, DIL and SOP packages Operating temperature range of -40 C to 85 C for HEF devices Extended Operating Temperature range of -45 C to 125 C for HEC devices
		* At Vcc = 15V



13

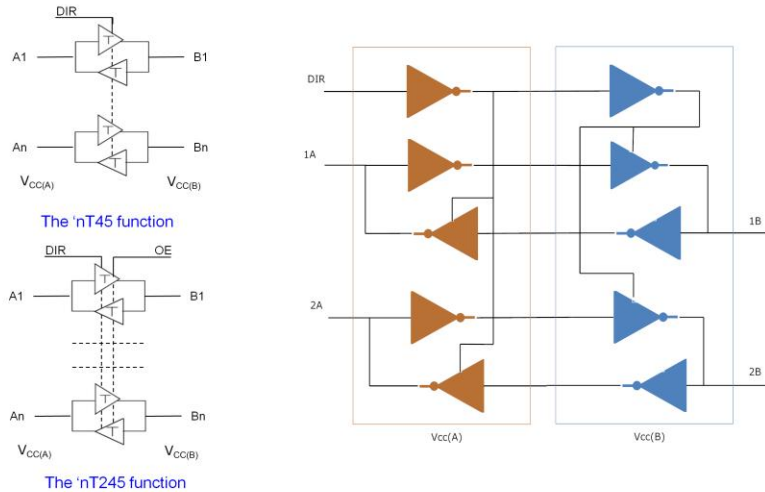
For high to low voltage translation HC/T, AHC/T and HEF4000B logic families offer different logic functions with over supply voltage tolerant inputs and built in Schmitt trigger for slower inputs. With TTL compatible inputs, some level of low to high voltage translation can also be achieved. Wide operating temperature range of -55C to 150C makes these devices ideal for use in systems designed for harsh weather conditions as well.

Family Specifications Comparison

ALVC	LVT	ALVT
<ul style="list-style-type: none"> • Vcc: 1.2V – 3.6V • High Speed (~ 2 ns prop delay) • Static output drive of ± 24 mA* • TTL compatible inputs • 5V Overvoltage tolerant I/Os in non bus hold parts • Suitable for mixed voltage 5V/3.3V/1.8V designs • 3 State Outputs • Flow Through Pin out** • Live Insertion and Bus Hold • Optional Termination Resistors • RoHS and Halogen free SO, SSOP and TSSOP and leadless DQFN packages • Operating Temperature Range of -40 C to 85 C 	<ul style="list-style-type: none"> • VCC : 2.7V – 3.6V • High Speed (~ 2 ns prop delay) • Static output drive of -32/64 mA* • TTL compatible inputs • 5V tolerant inputs • 3 State Outputs • Live Insertion and Bus Hold • Flow Through Pin out** • Optional Termination Resistors • RoHS and Halogen Free SO, SSOP, TSSOP and innovative leadless DQFN and LFBGA • Operating temperature range of -40 C – 85 C 	<ul style="list-style-type: none"> • VCC : 2.3V – 3.6V • High Speed (~1.5 ns prop delay) • Static output drive of -32/64 mA* • TTL compatible inputs • 5V tolerant inputs • 3 State Outputs • Live Insertion and Bus Hold • Flow Through pin out** • Optional Termination Resistors • RoHS and Halogen Free SSOP, TSSOP leadless BGA packages • Operating temperature range of -40 C – 85 C
<p>* At Vcc = 3V</p> <p>** For Voltage Translators and Transceivers functions Only</p>		
		14

ALVC logic is a high speed version of LVC logic with supply voltage range of 1.2V to 3.6V. LVT and ALVT are BiCMOS logic devices with drive currents as high as 64mA, suitable for high load applications. Outputs of LVT and ALVT devices can be tristated with output enable control and during power up and power down. Also the inputs of these devices are over voltage tolerant. These features provide an additional level of live insertion for LVT and ALVT voltage translators.

Dual Supply Voltage Translators for Low to High and High to Low Voltage Translation



15

These are the devices with two supply voltages and different voltage ranges. These translators can be used for uni or bidirectional voltage level translation. Some bidirectional voltage translators have a 'DIR' pin to control the direction of data while others have 'DIR' and 'Output Enable' pins for tristating the outputs and save power. Output enable control is available in 245 functions. Low to high as well as high to low voltage translation can be done with these devices.

NXP's Dual Supply Voltage Translators

Part Number	Description	Voltage range	Prop. Delay (ns)*	Package type	Package drawing
74AVC(H)1T45GM	single bit bi-directional translator (3-state)	0.8 V to 3.6 V	9.2	MicroPak 6L	SOT886
74AVC(H)1T45GW	single bit bi-directional translator (3-state)	0.8 V to 3.6 V	9.2	PicoGate 6L	SOT363
74AVC(H)2T45DP	dual bit bi-directional translator (3-state)	0.8 V to 3.6 V	9.2	PicoGate 8L	SOT505
74AVC(H)2T45GD	dual bit bi-directional translator (3-state)	0.8 V to 3.6 V	9.2	XSON8	SOT996-2
74AVC(H)2T45GT	dual bit bi-directional translator (3-state)	0.8 V to 3.6 V	9.2	MicroPak 8L	SOT833-1
74AVC(H)4T245DP	4-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	DHVQFN16	SOT763-1
74AVC(H)4T245GD	4-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	SO16	SOT109-1
74AVC(H)4T245GT	4-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	TSSOP16	SOT403-1
74AVC(H)8T245BQ	8-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	DHVQFN24	SOT815-1
74AVC(H)8T245PW	8-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	TSSOP24	SOT355-1
74AVC(H)16T245BQ	16-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	HUQFN60U	SOT1025-1
74AVC(H)16T245DGG	16-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	TSSOP48	SOT362-1
74AVC(H)16T245DGV	16-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	TVSOP48	SOT480-1
74AVC(H)16T245EV**	16-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	VFBGA56	SOT702-1
74AVC(H)20T245BQ	20-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	HUQFN60U	SOT1025-1
74AVC(H)20T245DGG	20-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	TSSOP56	SOT364-1
74AVC(H)20T245DGV	20-bit bi-directional translator (3-state)	0.8 V to 3.6 V	6.0	TVSOP56	SOT481-2
74LVC(H)1T45GF	single bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	MicroPak 6L	SOT891
74LVC(H)1T45GM	single bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	MicroPak 6L	SOT886
74LVC(H)1T45GW	single bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	PicoGate 6L	SOT363
74LVC(H)2T45GD	dual bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	XSON8	SOT996-2
74LVC(H)2T45GM	dual bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	MicroPak 8L	SOT902-1
74LVC(H)2T45GT	dual bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	MicroPak 8L	SOT833-1
74LVC(H)8T245BQ**	8-bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	DHVQFN24	SOT815-1
74LVC(H)8T245PW**	8-bit bi-directional translator (3-state)	1.2 V to 5.5 V	5.4	TSSOP24	SOT355-1
74AUP1T34GF	single bit uni-directional translator	1.1 V to 3.6 V	5.7	MicroPak 6L	SOT891
74AUP1T34GM	single bit uni-directional translator	1.1 V to 3.6 V	5.7	MicroPak 6L	SOT886
74AUP1T34GW	single bit uni-directional translator	1.1 V to 3.6 V	5.7	PicoGate 6L	SOT353-1
74AUP1T45GF	single bit bi-directional translator (3-state)	1.1 V to 3.6 V	6.5	MicroPak 6L	SOT891
74AUP1T45GM	single bit bi-directional translator (3-state)	1.1 V to 3.6 V	6.5	MicroPak 6L	SOT886
74AUP1T45GW	single bit bi-directional translator (3-state)	1.1 V to 3.6 V	6.5	PicoGate 6L	SOT363



* Typical value at 25 C, VCC(A) = min., VCC(B) = max. node voltage
 ** In Development

16

Dual supply voltage translators with 'DIR" pin are available from NXP in AVC, LVC, ALVC and AUP logic families. Output Enable feature is available in '245 functions offered in 4, 8, 16 and 20 bit devices. A wide voltage translation range of 0.8V to 5.5V can be addressed by using these devices.

Dual Supply Translators

Features and Benefits

- ▶ Wide voltage translation range for mixed 5.0 V/3.3 V/2.5 V/1.8 V/1.2 V designs
- ▶ Direction control input for bidirectional data flow
- ▶ High speed and low power consumption for battery operated and handheld systems
- ▶ Live insertion and extraction for systems which are always powered on
- ▶ 3 state outputs for high impedance suspend mode
- ▶ Flow through pin out for PCB lay out flexibility
- ▶ Bus hold function for less external components and no floating inputs
- ▶ Innovative leadless MicroPak and DQFN packages for space saving








17

Dual supply translators are available with various unique features that make them suitable for many different applications. Bidirectional data flow, flow through pin out, bus hold and live insertion are some of these features.

Voltage Translators: NXP Packages

Package suffix	GW	GW	GM	GT	GM	GD
	5-pin	6-pin	6-pin	8-pin	8-pin	8-pin
						
Package	SOT353	SOT363	SOT886	SOT833	SOT902	SOT996
Width (mm)	2.10	2.10	1.00	1.00	1.60	3.00
Length (mm)	2.00	2.00	1.45	1.95	1.60	2.00
Pitch (mm)	0.65	0.65	0.50	0.50	0.50	0.50

Package suffix	GF	DP	D	PW	BQ	PW
	6-pin	8-pin	16-pin	16-pin	16-pin	24-pin
						
Package	SOT891	SOT505	SOT109-1	SOT403-1	SOT763-1	SOT355-1
Width (mm)	1.00	3.00	6.00	6.40	2.50	6.40
Length (mm)	1.00	3.00	9.90	5.00	3.50	7.80
Pitch (mm)	0.35	0.65	1.27	0.65	0.65	0.65

Package suffix	BQ	DGG	DGV	DGG	DGV	BQ
	24-pin	48-pin	48-pin	56-pin	56-pin	60-pin
						
Package	SOT815-1	SOT362-1	SOT480-1	SOT364-1	SOT481-2	SOT1134
Width (mm)	3.5	8.1	6.4	8.1	6.4	4.0
Length (mm)	5.5	12.5	10.1	14.0	11.3	6.0
Pitch (mm)	0.5	0.5	0.4	0.5	0.4	0.5



18

Standard SO, SSOP and TSSOP packages are offered in addition to innovative smaller leadless MicroPak and DQFN packages for voltage translators from NXP. Packages from NXP are RoHS compliant with no lead and are also dark green with no halogen and antimony oxides for better safer environment.

Selection of Voltage Translator

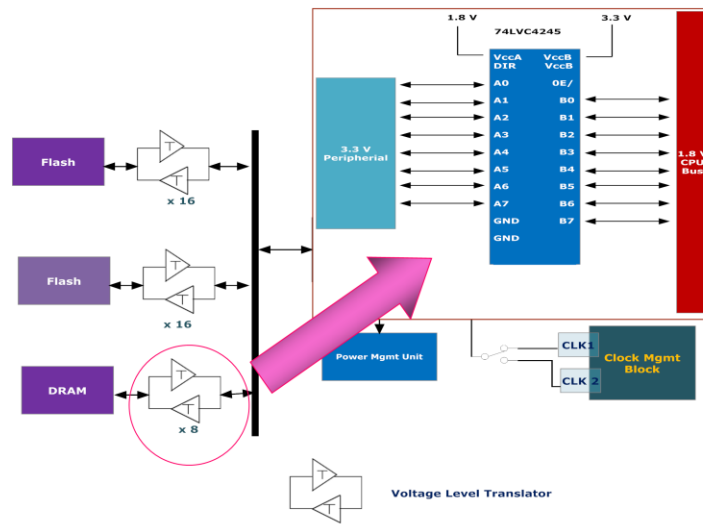
- Determine the number of channels or bits required.
- Determine the need for low to high or high to low voltage translation in application.
- Determine the direction of data flow between driver and receiver, it can be a bidirectional voltage translation as well
- Determine the required source or sink current, V_{oh} , V_{ol} , V_{ccA} , V_{ccB} and propagation delay
- For high to low voltage translation, choose a device with over-voltage tolerant inputs. (For interfacing with voltages far in excess of typical logic families (i.e 5V) choose devices with input clamping diodes and use current limiting resistors (automotive / industrial applications))
- For low to high voltage translation, choose a device with low threshold inputs or open-drain outputs
- For bi-directional or uni-directional data flow with high to low and low to high voltage translation, choose a dual supply transceiver/ translator



19

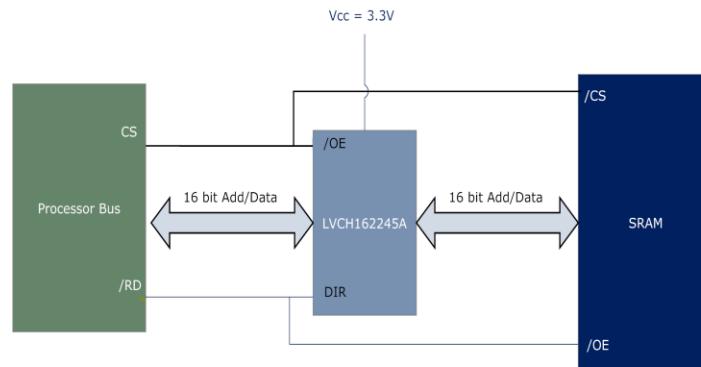
The slide provides helpful hints for selection of a right voltage translator in a system. Determination of number of channels, direction of data flow, translation voltage and current levels and required propagation delay are critical in selection of right voltage translator. With NXP's broad voltage translation portfolio, right voltage translator is always available for any application with specific operating requirements.

Application of Voltage Translator



An 8 bit, dual supply voltage level translator is used to translate the voltage signal levels from 1.8V CPU bus to 3.3V memory and vice versa.

Bidirectional voltage translation between Processor and Memory



21

The slide explains the use of LVCH162245A as a bidirectional voltage level translator between 3.3V processor bus and 5V SRAM with TTL compatible input levels. By default, processor writes the data on memory. Whenever, processor tries to read the SRAM, it will generate Chip Select first. Since there is bus hold at inputs of LVCH162245, address will be passing through the transceiver into SRAM data lines. After sometime processor bus will be tristated and it'll generate RD signal. While /OE is still low, SRAM starts transmitting data. Data from SRAM appears at B port at the same time as the DIR input goes from HIGH to LOW and data starts flowing from B to A port. Data flows from processor to SRAM since inputs of SRAM are TTL compatible. Data flow from SRAM to processor due to high to low voltage translation by using over supply voltage translation at LVC inputs. Also, LVCH162245 is designed with 30 Ohm series termination resistors in both HIGH and LOW output stages to reduce line noise and ensure better signal integrity in design with no reflections, undershoots or overshoots.

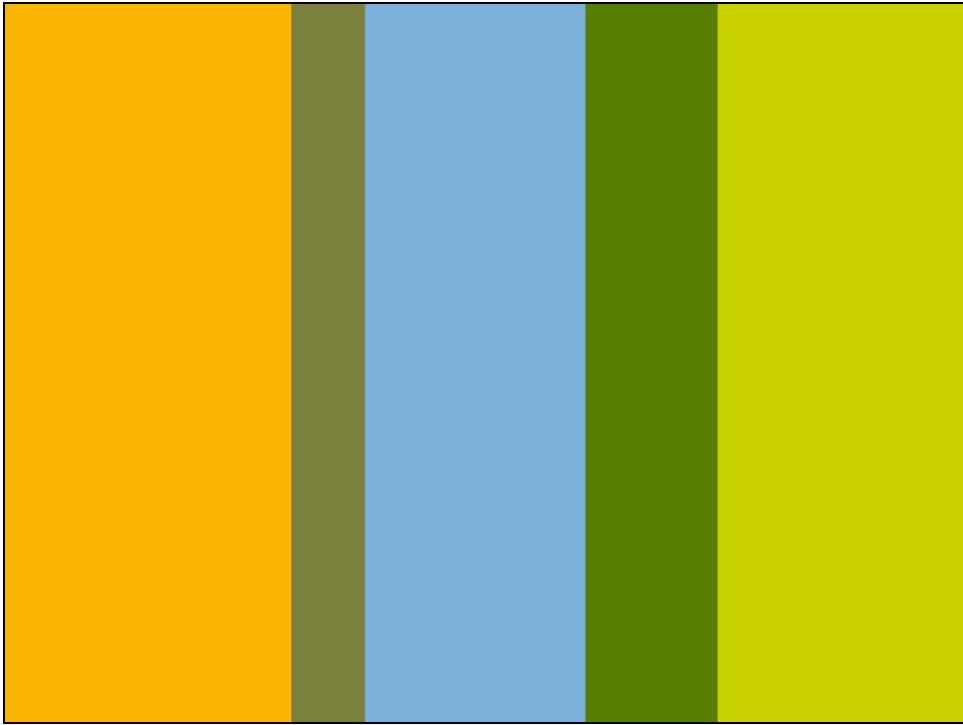
Summary

- ▶ Low to high and high to low voltage translation is required between driver and receiver devices in mixed supply voltage systems
- ▶ Over supply voltage tolerance, low input thresholds, clamp diodes at inputs and open drain outputs are some of the common techniques for voltage translation
- ▶ In addition to voltage translation feature in standard logic, NXP also offers dual supply uni and bidirectional voltage translators
- ▶ Availability of voltage translators in different logic families with different electrical specifications provides greater design flexibility
- ▶ Standard logic and innovative leadless packages are available for space critical boards
- ▶ Complete portfolio of NXP's voltage level translators can be found at <http://ics.nxp.com/support/techtips/voltage.level.translation/>



22

NXP offers a broad portfolio of voltage translators in various logic families with different electrical specifications and package options. These voltage translators can be used for low to high or high to low voltage level translation between driver and receiver at high speed with very low power consumption. Various standard and leadless packages are available for these devices that can be used to save PCB space significantly. For a complete portfolio offering of voltage translators, please visit www.standardics.nxp.com/products/voltage.translation



Thank You!